

1. General Description

The HG65C1R070F is a 650V, 70 mΩ Gallium Nitride (GaN) FET in a TO-220 package. It is a normally-off device that combines asiasemitech latest high-voltage GaN HEMT with a low voltage silicon MOSFET to offer superior reliability and performance.

2. Features and Benefits

- JEDEC-qualified GaN technology
- Dynamic $R_{DS(on)eff}$ production tested
- Wide gate safety margin
- Capable of reverse conduction
- Low gate charge
- RoHS compliant and Halogen-free packaging
- Achieves increased efficiency in both hard- and soft- switched circuits
 - Increased power density
 - Reduced system size and weight
 - Overall lower system cost
- Easy to drive with commonly-used gate drivers

3. Applications

- Industrial power supplies
- Telecom power
- Data center
- Consumer

4. Key Specifications

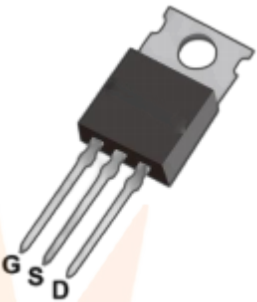
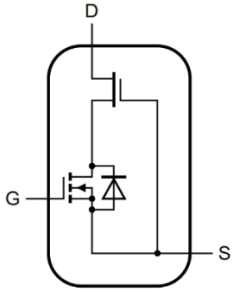
Table 1. Key Specifications

Symbol		Parameter	Value	Unit
$V_{DS, max}$		Drain-source voltage	650	V
$I_{D, max}$		Continuous drain current @Tc = 25°C	32	A
$R_{DS(on), typ}$		Drain-source on-state resistance	70	mΩ
Q_G, typ		Total gate charge	14	nC
$Q_{RR, typ}$		Reverse recovered charge	124	nC

650V, 70mΩ typ., Gallium Nitride (GaN) FET in TO-220

5. Pin Description

Table 2. Pin Description

Pin	Description	Top View	Graphic Symbol
G	Gate		
S	Source		
D	Drain		

6. Ordering Information

Table 3. Ordering Information

Part number	Package	Marking Code
HG65C1R070F	TO-220	65C1R070

7. Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings (Tc=25°C unless otherwise stated)

Parameter	Symbol	Min.	Max.	Unit.	Conditions
Drain to source voltage	V_{DSS}	650	-	V	$V_{GS} = 0V$
Transient drain to source voltage	$V_{DSS(TR)}$	-	800		Non-repetitive Pulse for $\leq 10ms$ at 25°C
Gate to source voltage	V_{GSS}	-20	20		
Maximum power dissipation	P_D	-	156	W	$T_c = 25^\circ C$, Fig.1
Continuous drain current	I_D	-	32	A	$T_c = 25^\circ C$
		-	20	A	$T_c = 100^\circ C$
Pulsed drain current	I_{DM}	-	95	A	Pulse width t_p limited by $T_{J,max}$
Operating temperature	T_J	-55	150	°C	
Storage temperature	T_S	-55	150	°C	

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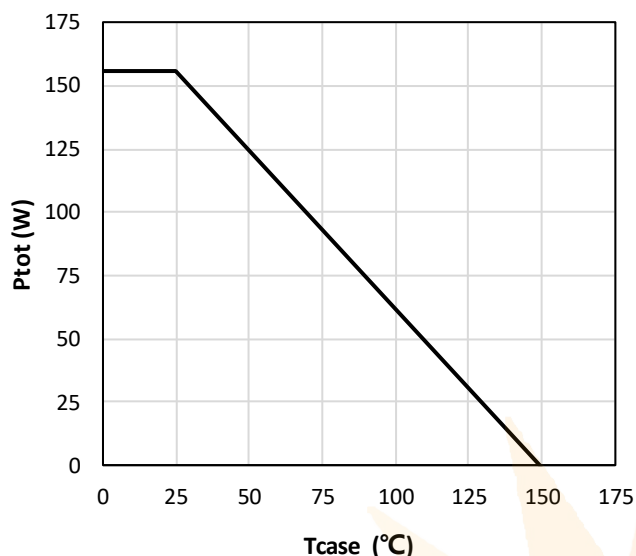


Fig. 1. Power Dissipation

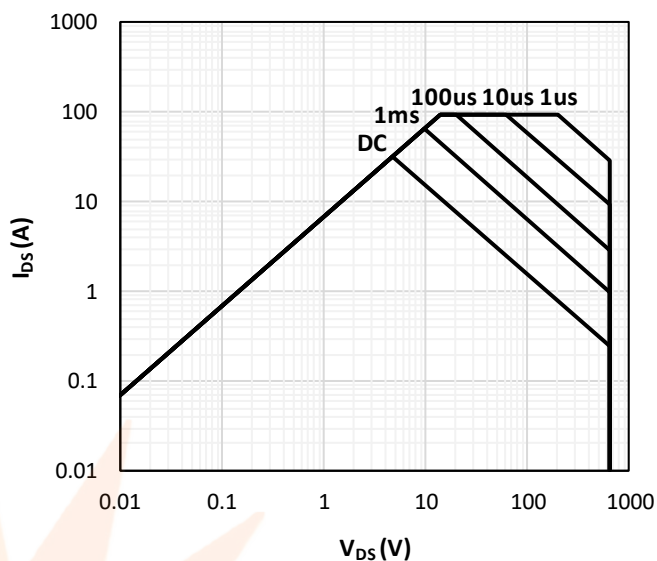


Fig 2. Safe Operating Area $T_C = 25^\circ\text{C}$

8. Thermal Characteristics

Table 5. Thermal Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Thermal resistance (Junction-to-case)	$R_{th(j-c)}$	-	-	0.8	$^{\circ}C/W$	
Thermal resistance (Junction-to-ambient)	$R_{th(j-a)}$	-	-	50	$^{\circ}C/W$	
Soldering peak temperature	T_{SOLD}	-	-	260	$^{\circ}C$	1.6mm (0.063 in.) from case for 10s

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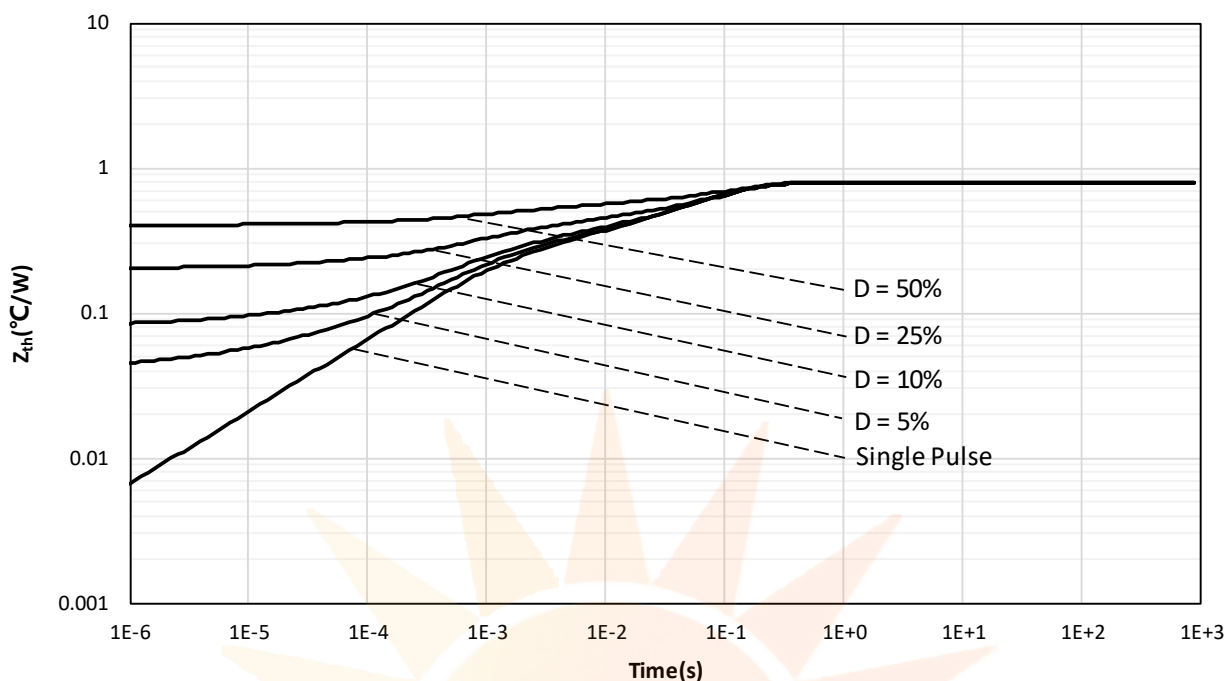


Fig. 3. Transient Thermal Impedance

9. Electrical Characteristics

Table 6. Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Device Characteristics						
Gate threshold voltage	$V_{GS(th)}$	2.9	3.7	4.5	V	$V_{DS} = V_{GS}$, $I_D = 0.5mA$, $T_J = 25^\circ C$
		-	2.8	-		$V_{DS} = V_{GS}$, $I_D = 0.5mA$, $T_J = 150^\circ C$
Drain-source on-state resistance ^a	$R_{DS(on)}$	-	70	87.5	mΩ	$V_{GS} = 12V$, $I_D = 18A$, $T_J = 25^\circ C$, Fig.18 , Fig.19
		-	147	-		$V_{GS} = 12V$, $I_D = 18A$, $T_J = 150^\circ C$, Fig.18 , Fig.19
Drain-to-source leakage current	I_{DSS}	-	4.5	22.5	μA	$V_{DS} = 650V$, $V_{GS} = 0V$, $T_J = 25^\circ C$
		-	36	-		$V_{DS} = 650V$, $V_{GS} = 0V$, $T_J = 150^\circ C$
Gate-to-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS} = 20V$, $V_{DS} = 0V$, $T_J = 25^\circ C$
		-	-	-100		$V_{GS} = -20V$, $V_{DS} = 0V$, $T_J = 25^\circ C$

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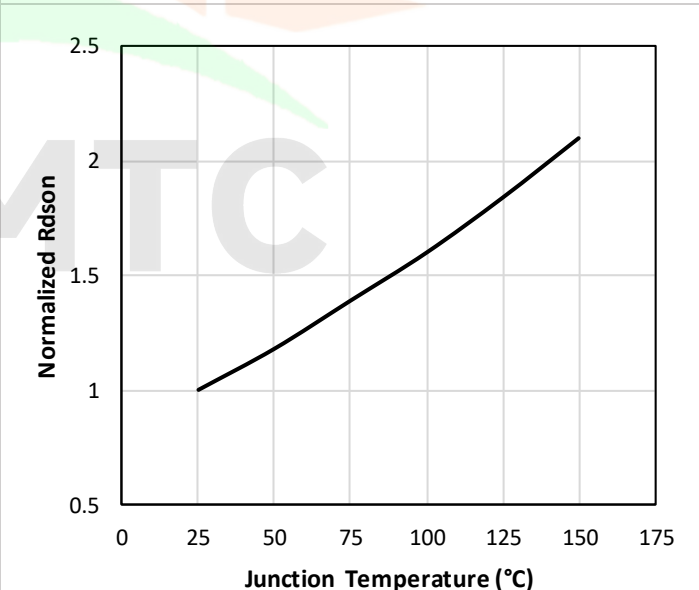
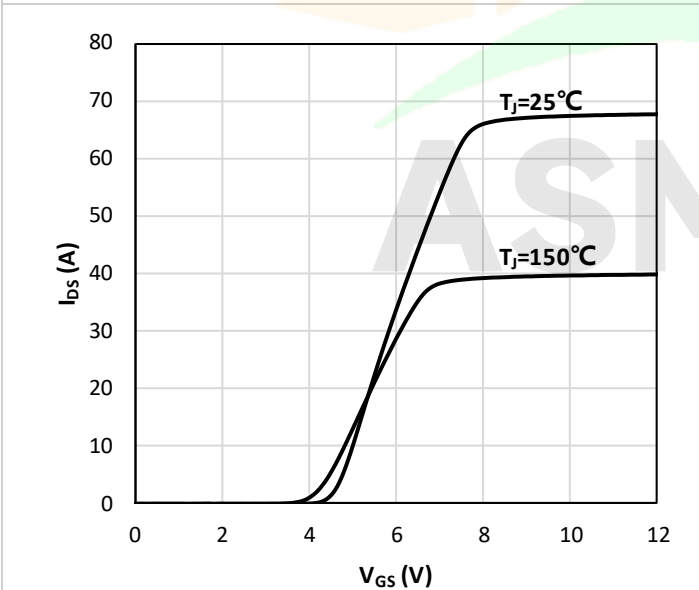
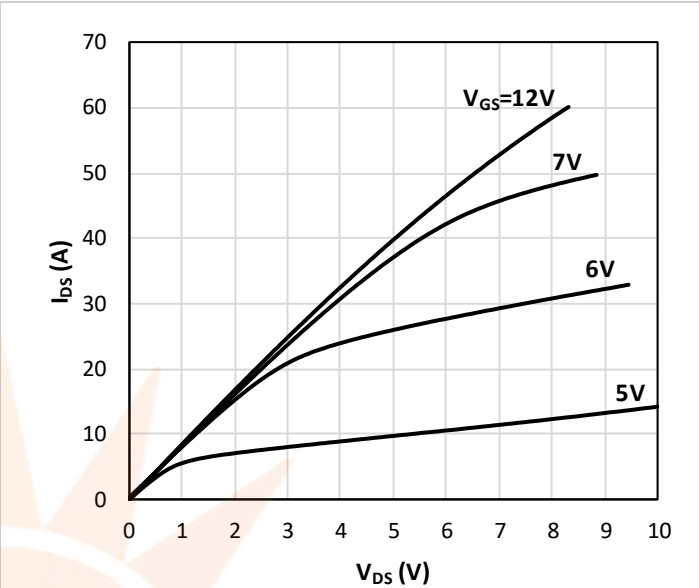
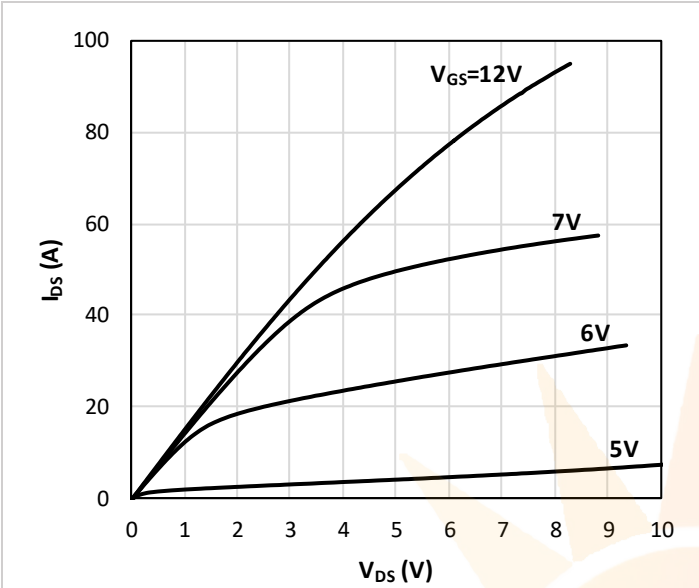
Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions
Input capacitance	C _{ISS}	-	750	-	pF	V _{GS} = 0V, V _{DS} = 400V, f = 1MHz, Fig.8
Output capacitance	C _{OSS}	-	60	-		
Reverse transfer capacitance	C _{RSS}	-	0.4	-		
Output capacitance, energy related ^b	C _{O(er)}	-	110	-	pF	V _{GS} = 0V, V _{DS} = 0V to 400V, Fig.9 , Fig.10
Output capacitance, time related ^c	C _{O(tr)}	-	220	-		
Total gate charge	Q _G	-	14	-	nC	V _{DS} = 400V, V _{GS} = 0V to 12V, I _D = 16A, Fig.11
Gate-source charge	Q _{GS}	-	3.4	-		
Gate-drain charge	Q _{GD}	-	3.9	-		
Output charge	Q _{OSS}	-	88	-	nC	V _{GS} = 0V, V _{DS} = 0V to 400V
Turn-on delay	t _{D(on)}	-	23	-	ns	V _{DS} = 400V, V _{GS} = 0V to 12V, I _D = 18A, R _G = 51Ω, Z _{FB} = 240Ω at 100MHz, Fig.14 , Fig.15
Rise time	t _R	-	15	-		
Turn-off delay	t _{D(off)}	-	58	-		
Fall time	t _F	-	11	-		
Reverse Device Characteristics						
Reverse voltage ^d	V _{SD}	-	2	-	V	V _{GS} = 0V, I _S = 18A, Fig.12
		-	1.4	-		V _{GS} = 0V, I _S = 9A, Fig.12
Reverse recovery time	t _{RR}	-	30	-	ns	I _S = 18A, V _{DD} = 400V, di/dt = 1000A/us, Fig.16 , Fig.17
Reverse recovery charge	Q _{RR}	-	124	-	nC	

Notes:

- Dynamic $R_{DS(on)}$ value
- Equivalent capacitance to give same stored energy from $0V$ to $400V$
- Equivalent capacitance to give same charging time from $0V$ to $400V$
- Includes dynamic $R_{DS(on)}$ effect

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9.1 Electrical characteristics(curves) (T_C=25°C unless otherwise stated)



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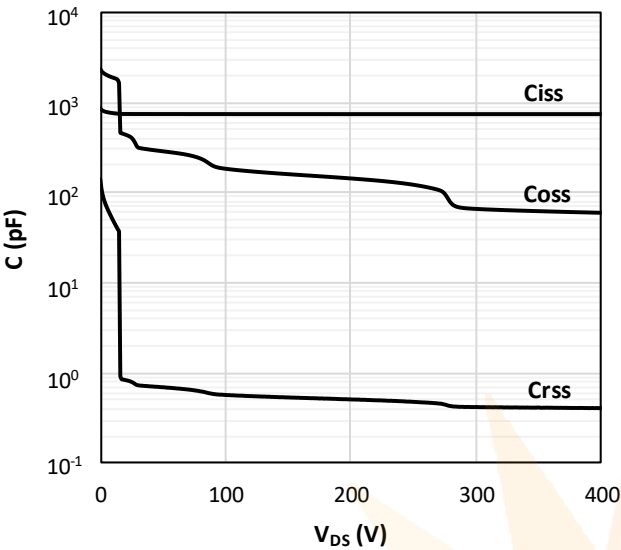


Fig. 8. Typical Capacitance
 $V_{GS} = 0V, f = 1MHz$

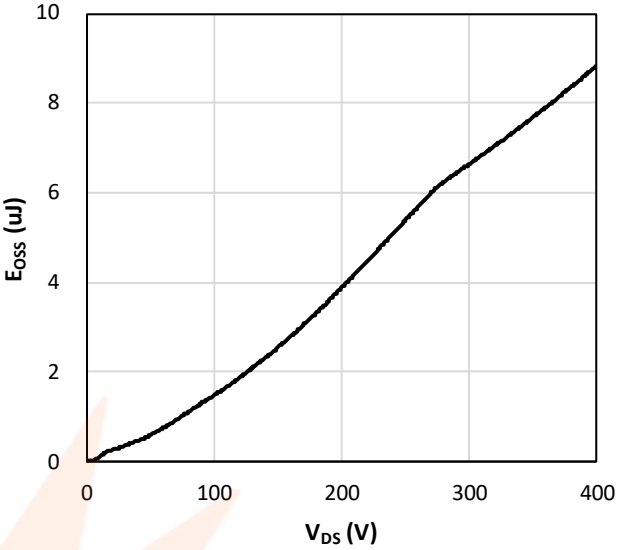


Fig. 9. Typical C_{oss} Stored Energy
 $V_{GS} = 0V, f = 1MHz$

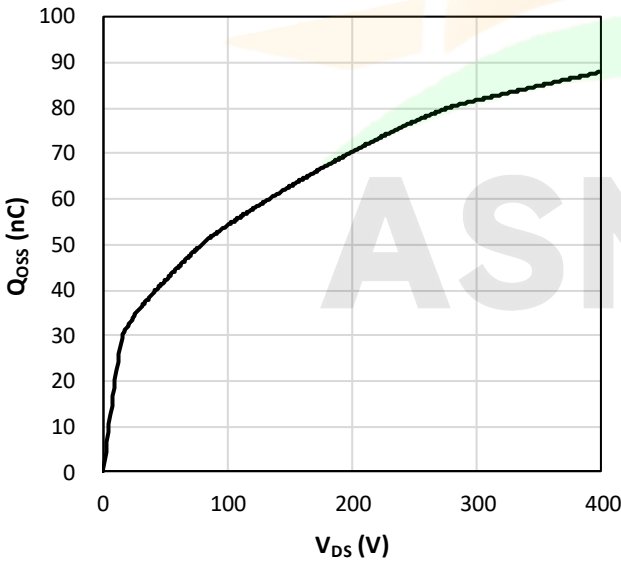


Fig. 10. Typical Q_{oss}

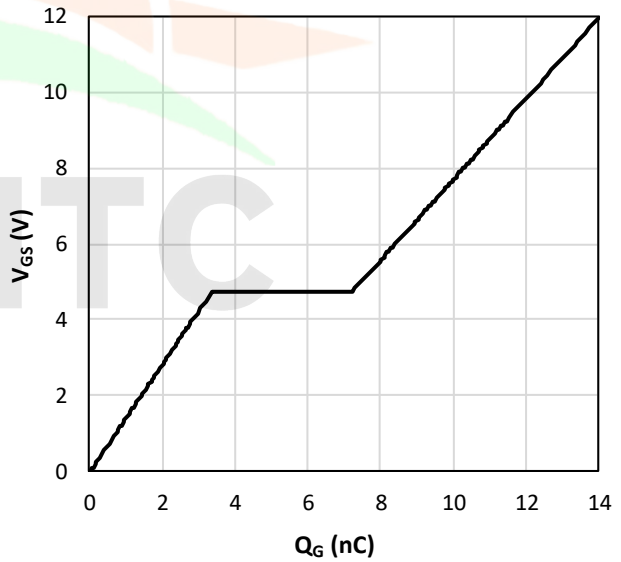


Fig. 11. Typical Gate Charge
 $I_{DS} = 18A, V_{DS} = 400V$

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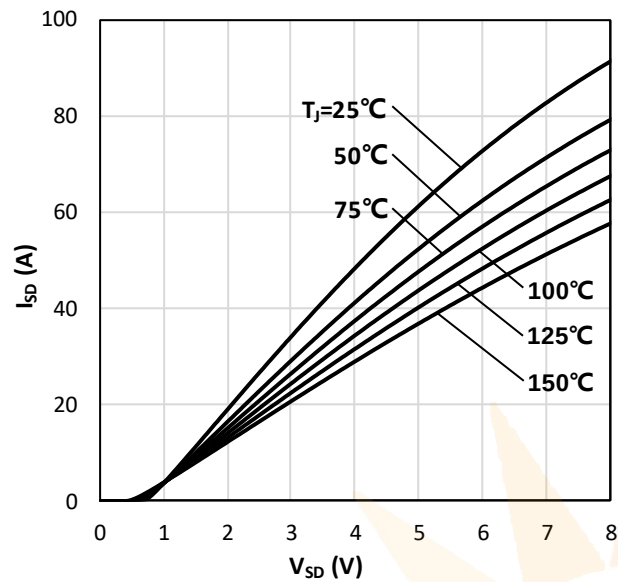


Fig. 12. Forward Characteristics of Rev. Diode

$I_{SD} = f(V_{SD})$

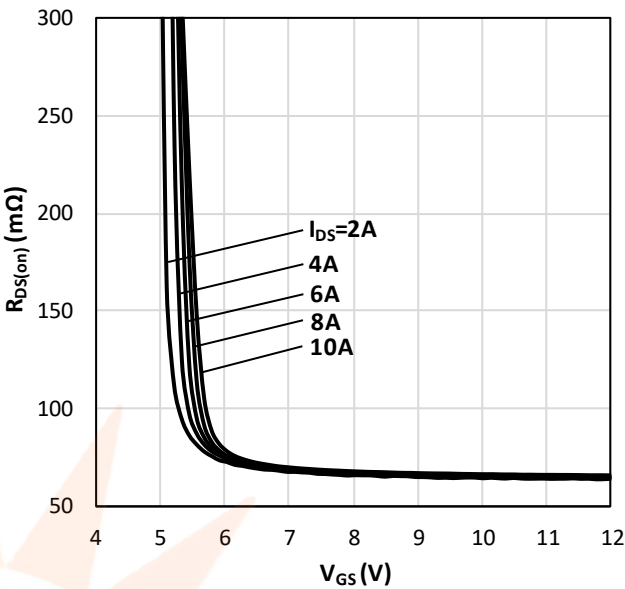


Fig. 13. Typical $R_{DS(on)}$

10. Test Circuits

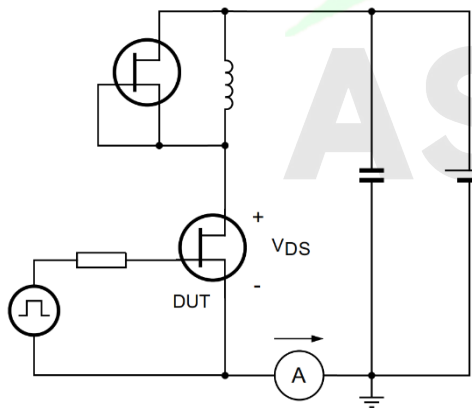


Fig. 14. Switching Time Test Circuit

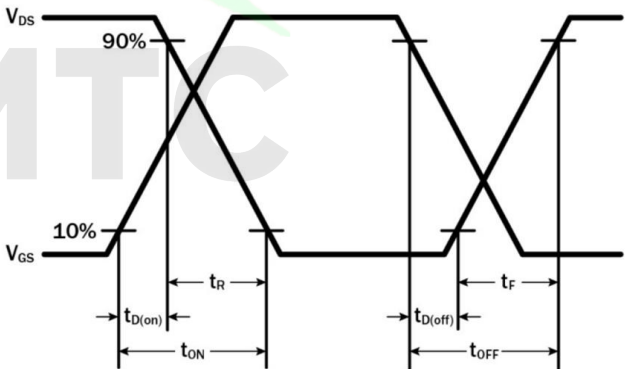


Fig. 15. Switching Time Waveform

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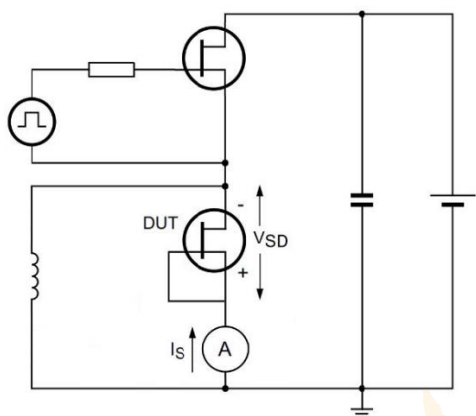


Fig. 16. Diode Characteristics Test Circuit

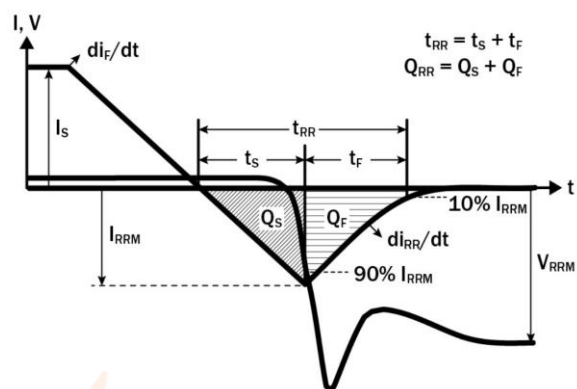


Fig. 17. Diode Recovery Waveform

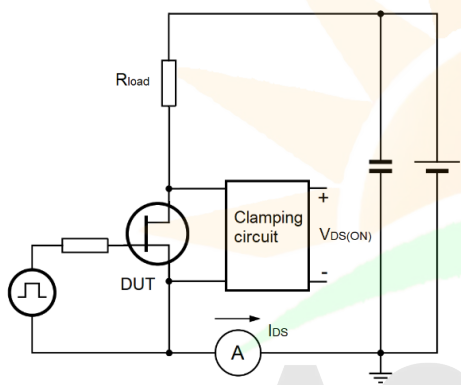


Fig. 18. Dynamic $R_{DS(on)eff}$ Test Circuit

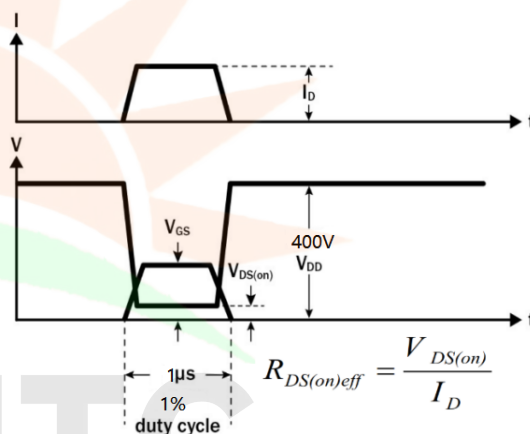


Fig. 19. Dynamic $R_{DS(on)eff}$ Waveform

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11. Package Information

11.1 TO-220 Package Information

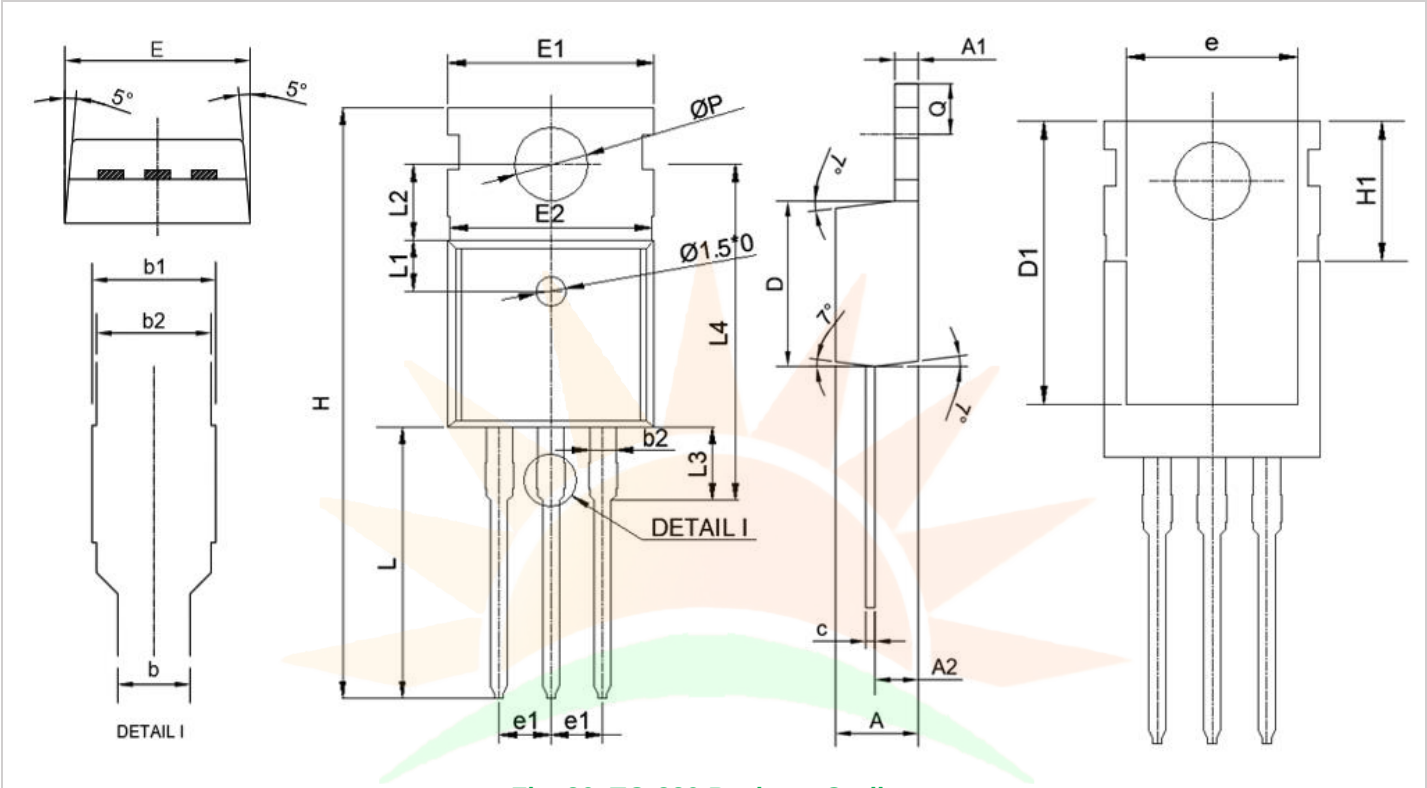


Fig. 20. TO-220 Package Outline

SYMBOL	MIN	NOM	MAX	SYMBOL	MIN	NOM	MAX
A	4.56	4.57	4.58	e	7.50	8.00	8.40
A1	1.28	1.3	1.32	e1	2.53	2.54	2.55
A2	2.3	2.4	2.5	H	28.8	29	29.2
b	0.7	0.8	0.9	H1	6.4	6.5	6.6
b1	1.27	1.37	1.47	L	13.05	13.35	13.65
b2	1.26	1.27	1.28	L1	2.4	2.5	2.6
c	0.45	0.5	0.6	L2	3.6	3.7	3.8
D	9.14	9.15	9.16	L3	2.92	3	3.08
D1	13.2	13.21	13.22	L4	15.82	15.9	15.98
E	9.95	10.05	10.15	Q	2.73	2.8	2.87
E1	10.0	10.05	10.1	P	3.6	-	3.65
E2	9.87	9.88	9.89				

12. Important Notice

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Revision History

Revision	Date	Changes
1.0	29/01/2024	Release Preliminary Datasheet

